What is claimed is:

1. A memory device with multiple bits per cell, comprising:

a side electrode;

a doped semiconductor region disposed laterally in contact with a sidewall of the side electrode, such that the doped semiconductor region forms a diode, or the junction between the side electrode and the doped semiconductor region forms a diode;

a layer of phase-changing material disposed laterally in contact with a sidewall of the doped semiconductor region, such that the doped semiconductor region is disposed between the layer of phase-changing material and the side electrode; and

an upper electrode disposed on the layer of phase-changing material.

2. The memory device as claimed in claim 1, wherein the doped semiconductor region forms a diode.

3. The memory device as claimed in claim 2, wherein the doped semiconductor region is a PN junction diode.

4. The memory device as claimed in claim 3, wherein the side electrode is metal.

5. The memory device as claimed in claim 4, wherein the side electrode is a tungsten plug.

6. The memory device as claimed in claim 1, wherein the junction between the side electrode and the doped semiconductor region forms a diode.

7. The memory device as claimed in claim 6, wherein the side electrode is doped polysilicon having a different conductive type from the doped semiconductor region to form a PN junction diode with the doped semiconductor region.

8. The memory device as claimed in claim 7, wherein the side electrode is a doped polysilicon plug.

9. The memory device as claimed in claim 6, wherein the side electrode is metal to form a Schottky diode with the doped semiconductor region.

10. The memory device as claimed in claim 9, wherein the side electrode is a tungsten plug.

11. The memory device as claimed in claim 1, wherein the phase-changing material is a chalcogenide material.

12. The memory device as claimed in claim 1, wherein the upper electrode is metal.

13. The memory device as claimed in claim 1, wherein the doped semiconductor region has a thickness of 10 Å to 1500 Å.

14. The memory device as claimed in claim 13, wherein the doped semiconductor region has a thickness of 100 Å to 1000 Å.

15. A memory device with multiple bits per cell, comprising:

a first side electrode;

a second side electrode; and

a storage region laterally disposed between the first and second side electrodes,

wherein the storage region includes:

a first doped semiconductor region disposed laterally in contact with a sidewall of the first side electrode, such that the first doped semiconductor region forms a diode, or the junction between the first side electrode and the first doped semiconductor region forms a diode;

a second doped semiconductor region disposed laterally in contact with a sidewall of the second side electrode, such that the second doped semiconductor region forms a diode, or the junction between the second side electrode and the second doped semiconductor region forms a diode;

a layer of phase-changing material disposed laterally between and in contact with the first and second doped semiconductor regions; and

an upper electrode disposed on the layer of phase-changing material.

16. The memory device as claimed in claim 15, wherein the memory device includes:

a first side electrode;

a second side electrode; and

a plurality of the storage regions disposed between the first and second side electrodes, stacked vertically, and separated from each other by a dielectric layer.

17. A process for fabricating a memory device with multiple bits per cell, comprising the following steps:

(a) forming a conductive layer on a semiconductor substrate;

(b) forming a dielectric layer on the conductive layer;

(c) forming a doped semiconductor structure on the dielectric layer;

(d) forming an insulating layer on the doped semiconductor structure and the dielectric layer;

(e) selectively removing the insulating layer downwardly to the underlying doped semiconductor structure to expose the dielectric layer and to separate the doped semiconductor structure into two doped semiconductor regions, thus forming a trench;

(f) forming a layer of phase-changing material in the trench;

(g) forming an upper electrode on the layer of phase-changing material;

(h) planarizing the upper electrode and the layer of phase-changing material to stop on the insulating layer;

(i) repeating steps (b) to (h) N times to form (N+1) levels of dielectric layers, doped semiconductor regions, insulating layers, layers of phase-changing material, and upper electrodes, wherein N is an integer equal to or greater than 0;

(j) selectively removing (N+1) levels of insulating layers and dielectric layers to expose the sides of the (N+1) levels of doped semiconductor regions and the top surface of the conductive layer, forming two openings; and

(k) filling the two openings with a conductive material to form two conductive plugs,

wherein each of the doped semiconductor regions forms a diode, or the junction between the conductive plug and the doped semiconductor region forms a diode.

18. The process as claimed in claim 17, wherein each of the doped semiconductor regions forms a diode.

19. The process as claimed in claim 18, wherein each of the doped semiconductor regions is a PN junction diode.

20. The process as claimed in claim 19, wherein the conductive plug is metal.

21. The process as claimed in claim 20, wherein the conductive plug is tungsten.

22. The process as claimed in claim 17, wherein the junction between the conductive plug and the doped semiconductor region forms a diode.

23. The process as claimed in claim 22, wherein the conductive plug is doped polysilicon having a different conductive type from the doped semiconductor region to form a PN junction diode.

24. The process as claimed in claim 22, wherein the conductive plug is metal to form a Schottky diode with the doped semiconductor region.

25. The process as claimed in claim 24, wherein the conductive plug is tungsten.

26. The process as claimed in claim 17, wherein the phase-changing material is a chalcogenide material.

27. The process as claimed in claim 17, wherein the upper electrode is metal.

28. The process as claimed in claim 17, wherein the doped semiconductor region has a thickness of 10 Å to 1500 Å.

29. The process as claimed in claim 28, wherein the doped semiconductor structure has a thickness of 100 Å to 1000 Å.